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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/750,342 | 12/29/2000 | Sung-II Park | 3430-0165P | 6907 |
| 7590 | 10/21/2003 | | EXAMINER | |
| BIRCH, STEWART, KOLASCH & BIRCH, LLP | | | DUONG, THOI V | |
| P. O. Box 747 | | | ART UNIT | PAPER NUMBER |
| Falls Church, VA 22040-0747 | | | 2871 | |
| DATE MAILED: 10/21/2003 | | | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | |
|------------------------------|--------------------------|------------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 09/750,342 | PARK ET AL. |
| | Examiner Thoi V Duong | Art Unit 2871 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 11 August 2003.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-14 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) 5-13 is/are allowed.
 6) Claim(s) 1-4 and 14 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 11) The proposed drawing correction filed on 11 August 2003 is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.
 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

| | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input checked="" type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to the RCE, Paper No. 10, filed August 11, 2003.

Accordingly, claims 1, 5, 10, 12 and 14 were amended. Currently, claims 1-14 are pending in this application. Note that claims 5-13 have been allowed from the last office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 stand rejected under 35 U.S.C. 102(b) as being anticipated by Shiba et al. (USPN 5,684,555).

As shown in Figs. 1-4, Shiba discloses a liquid crystal display device comprising: upper and lower substrates 500 and 200 with a liquid crystal layer 600 interposed therebetween;

a sealant 113 between the upper and lower substrates in an area near an edge of the upper substrate 500;

a plurality of source pads 761-764 (Fig. 3) and gate pads (not shown) on the lower substrate 200;

a plurality of gate lines Y_{ij} and data lines X_i on the lower substrate (col. 3, line 56 through col. 4, line 8), each gate line being electrically connected with the

corresponding gate pad, each data line being electrically connected with the corresponding source pad (col. 4, lines 57-65);

a gate insulating layer 211 between the gate lines and the data lines;

a source PCB 800 and a gate PCB 900 electrically connected with the plurality of source pads and the plurality of gate pads, respectively, the source PCB 800 and the gate PCB 900 being formed along a first side 201a and a second side 201c, respectively, of the lower substrate and outside the area 111 in which the sealant 113 is formed such that the upper substrate is not formed over the source PCB or the gate PCB (see Fig. 1);

a plurality of transmitting wires 123-1 to 123-4 on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant (col. 5 line 67 through col. 6, line 5) such that the source PCB and the gate PCB are electrically connected to a counter electrode 541 via the power supply pads 731-738, wherein the power supply pad 734 is arranged in the vicinity of the corner of the lower substrate (col. 5, lines 29-42 and col. 6, lines 43-46); and

a plurality of switching devices 221,

wherein each transmitting wire has 5 narrow lines which are guided across the sealing area 111 (col. 6, lines 7-16).

Finally, Shiba discloses that, depending on the kind of the TFTs, the transmitting wires can be formed in the same step of forming the gate lines (col. 6, lines 33-35).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Shiba et al. (USPN 5,684,555) in view of Kuwashiro (USPN 5,945,984).

Shiba discloses a LCD device that is basically the same as that recited in claim 4 except for a plurality of dummy pads between the adjacent gate pads and between the adjacent source pads. As shown in Fig. 3, Kuwashiro discloses a LCD device in which dummy pads 731-1, 731-2 are disposed between data pads 721 for inspecting and repairing the display. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD device of Zhang with the teaching of Kuwashiro by forming a plurality of dummy pads between the adjacent gate pads and between the adjacent source pads so as to easily perform an inspection and repair the display.

6. Claim 14 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (USPN 5,995,189) in view of Noritake et al. (USPN 6,400,438 B1).

As shown in Figs. 1-6, Zhang discloses a method of fabricating a liquid crystal display device, the method comprising:

preparing first and second substrates;

forming a plurality of gate lines 106, gate pads (in scanning line drive circuit 104, gate transmitting lines 109 and dummy patterns 301 on the first substrate 201 (col. 6, lines 63-67, col. 7, lines 1-6, and col. 10, line 64 through col. 11, line 4);

forming a gate insulating layer 220 on the gate lines, gate pads, gate transmitting wires, and dummy patterns;

forming a plurality of data lines 105 and data pads (in signal line drive circuit 103), on the gate insulating layer;

forming a passivation layer 227 on the data lines and the data pads;

forming a sealant 107 on the first substrate (col. 11, lines 49-59), wherein the gate transmitting wires 109 connect the gate pads 104 to the source pads 103 across the sealant 107 via an external terminal 108 in the vicinity of a corner of the first substrate 101 as shown in Fig. 1 (col. 6, lines 51-59);

attaching the first and second substrates and forming a liquid crystal layer between the first and second substrates (col. 6, lines 44-50).

Zhang discloses a method of fabricating a liquid crystal display device that is basically the same as that recited in claim 14 except for scribing and breaking the second substrate. Referring to Fig. 5(a), Noritake discloses that insulator substrates 12a-12d are cut away by means of scribing and breaking a mother glass board 31 along the dotted line in Fig. 5(a) wherein the edges of the contact portions 22 of an opposite electrode 17 (Fig. 6) do not extend beyond or to the borders of the substrates 12a-12d and each separated substrate 12 is used to fabricate a LCD as shown in Fig. 6 (col. 3, lines 62-67 and col. 4, lines 1-8). Thus, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to modify the method of fabricating a LCD device of Zhang with the teaching of Noritake by scribing and breaking the second substrate so as to create separated liquid crystal panels without contaminants and hence improve reliability of the display (col. 4, lines 14-17).

Response to Arguments

7. Applicant's arguments filed 08/11/2003 have been fully considered but they are not persuasive.

With respect to claims 1 and 4, Applicant argued that Shiba et al. and Kuwashiro do not teach or suggest a source PCB and a gate PCB being formed along a first side and a second side, respectively, of the lower substrate and outside the area in which the sealant is formed, such that the upper substrate is not formed over the source PCB or the gate PCB, wherein the first and second sides meet at a corner of the lower substrate and a plurality of transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB in the vicinity of the corner of the lower substrate. The Examiner disagrees with the Applicant's remarks since, as shown in Figs. 1-4, Shiba et al. discloses a source PCB 800 and a gate PCB 900 being formed along a first side 201a and a second side 201c, respectively, of the lower substrate 200 and outside the area 111 in which the sealant 113 is formed, such that the upper substrate 500 is not formed over the source PCB or the gate PCB, wherein the first and second sides meet at a corner of the lower substrate and a plurality of transmitting wires 123-1 to 123-4 being electrically connected with the source pads (same connection for gate pads which are

not shown) across the sealant 113 such that the source PCB is electrically connected with the gate PCB via power pad 734 arranged in the vicinity of the corner of the lower substrate 200. Thus, Shiba et al. does teach all the limitations recited in claim 1. Meanwhile, Kuwashiro is relied on for teaching of disposing dummy pads between data pads to inspect and repair the display.

With respect to claim 14, Applicant argued that Zhang et al. and Noritake et al. do not teach forming a sealant on a first substrate, wherein the gate transmitting wires connect the gate pads to the source pads across the sealant in the vicinity of a corner of the first substrate. The Examiner disagrees with the Applicant's remarks because, as clearly shown in Fig. 1, Zhang et al. discloses a sealant 107 formed on a first substrate 101, wherein the gate transmitting wires 109 connect the gate pads to the source pads across the sealant via an external terminal 108 in the vicinity of a corner of the first substrate (upper left corner of Fig. 1). Thus, Zhang et al. does teach the limitations recited in claim 14. And Noritake et al. is relied on for teaching of insulating substrates which are cut away by scribing and breaking of a mother glass board.

Allowable Subject Matter

8. Claims 5-13 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claim 5, none of the prior art of record discloses, in combination with other limitations as claimed, a *repair wire crossing with each gate transmitting wire with the gate insulating layer interposed between the repair wire and the gate transmitting wire*.

Re claim 10, none of the prior art of record discloses, in combination with other limitations as claimed, *first and second repair wires, the first repair wire crossing with each of the source pads with the gate insulating layer interposed therebetween, the second repair wire crossing with each of the gate pads with the gate insulating layer interposed therebetween;*

Re claim 12, none of the prior art of record discloses, in combination with other limitations as claimed, *first and second dummy patterns on the lower substrate, the first dummy pattern being positioned along a first edge of the upper substrate, the second dummy pattern being positioned along a second edge of the upper substrate, the each dummy pattern having at least the same height as the gate transmitting wire.*

The most relevant references, USPN 5,684,555 of Shiba et al. and USPN 5,995,189 of Zhang, fail to disclose or suggest a liquid crystal display comprising a source PCB and a gate PCB electrically connected with the plurality of source pads and the plurality of gate pads, respectively, the source PCB and the gate PCB being formed outside the area in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB; a plurality of transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB; a repair wire crossing with each gate transmitting wire with the gate insulating layer interposed between the repair wire and the gate transmitting wire; and first and second dummy patterns on the lower substrate, wherein each dummy pattern has at least the same height as the gate transmitting wire. The Shiba's reference only discloses a liquid crystal display device

comprising a source PCB and a gate PCB electrically connected with the plurality of source pads and the plurality of gate pads, respectively, the source PCB and the gate PCB being formed outside the area in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB, and a plurality of transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrical connected with the gate PCB. Meanwhile, the Zhang's reference discloses a repair wire crossing with each gate transmitting wire with the gate insulating layer interposed between the repair wire and the gate transmitting wire, and first and second dummy patterns on the lower substrate, wherein each dummy pattern has at least the same height as the gate transmitting wire; however, the source PCB and the gate PCB are formed inside the area in which the sealant is formed.

Re claims 6 and 9, none of the prior art of record discloses, in combination with other limitations as claimed, *a repair wire with a specific resistance of 10 micro-ohm/cm including first and second closed roofs, the first closed roof being formed along first edge of the upper substrate, the second closed roof being formed along second edge of the upper substrate.*

The most revelant reference, USPN 5,995,189 of Zhang, fails to disclose or suggest that repair wire with closed roofs formed along the first and second edges of the upper substrate. The Zhang's reference reference only discloses a repair wiring pattern without closed roofs formed across the sealant on the lower substrate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

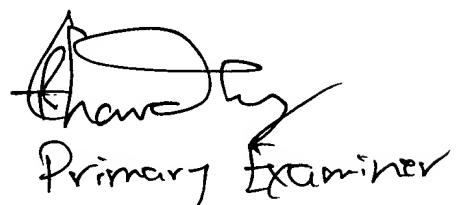
Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (703) 308-3171. The examiner can normally be reached on Monday-Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (703) 305-3492.

Thoi Duong

10/08/2003



Thoi Duong
Primary Examiner